IN THE SPECIFICATION:

Please amend the first full paragraph appearing on page 2 as follows.

This application is a ~~divisional~~ continuation of ~~US~~ U.S. Patent Application Serial No. 09/143,289, filed on August 28, 1998, titled "PLASMA TREATMENT OF AN INTERCONNECT SURFACE DURING FORMATION OF AN INTERLAYER ~~DIELECTRIC",~~ DIELECTRIC," now U.S. Patent No. 6,150,257, issued November 21, 2000, which is incorporated herein by reference.

Please amend the second full paragraph appearing on page 12 as follows:

Upper surface 16 as seen in Figure 3, may be formed by such methods as CMP or an anisotropic etchback that has an etch recipe selectivity that is substantially the same for interconnect 12 as for dielectric layer 14. By "substantially the ~~same",~~ same," it is meant that selectivity favors leaving dielectric layer 14, and favors it over interconnect 12 in a range from about 1.5:1, preferably about 1.2:1, more preferably 1.1:1, and most preferably 1.05:1.